Electronic Version
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HIGH PERFORMANCE FET WITH LATERALLY THIN EXTENSION

Abstract

field effect transistor (FET), integrated circuit (IC) chip including the FETs and a method of forming the FETs. The FETs have a device channel and a gate above the device channel with a doped source/drain extension at said each end of the thin channel. A portion of a low resistance material layer (e.g., a silicide layer) is disposed on source/drain extensions. The portions on the doped extensions laterally form a direct contact with the doped source/drain extension. Any low resistance material layer on the gate is separated from the low resistance material portions on the source/drain extensions.